a fifth step of calculating a difference between said pass value and said fail value after a processing in said fourth step is completed, and giving a command to repeat the processing from said second step onward until this difference is equal to or less than a measurement resolution.

REMARKS

Reconsideration is respectfully requested.

Claims 1-5 are pending in this application. Claim 4 is amended.

The Examiner objects to the Abstract. A new abstract is presented herewith, with attention to the points the Examiner asked to be changed.

The Examiner rejected claims 4 and 5 as being indefinite under 35 U.S.C. §112, 2nd paragraph. Applicant respectfully traverses the rejection. The Examiner asserts that claims 4 and 5 are indefinite alleging that "it is unclear if the 'said pass value' and the 'said fail value' [from the fifth step of claim 4] are the upper and lower limits of the test range, as noted in claim 4, first step, or if they are the 'said pass value' and 'said fail value', as noted in claim 4, fourth step." Applicant respectfully believes this is not indefinite.

The terms, "pass value" and "fail value" are used in a consistent manner throughout the claim. They are variable values that are initially set in the first step of claim 4 and may subsequently be re-set (or changed) in the fourth step if their

associated condition, as specified in the fourth step, is met. Specifically, "if the measurement result obtained in said third step is a pass", then the pass value variable is set to the measurement position set in the second step, and "if the measurement result obtained in said third step is a fail", then the fail value variable is set to the measurement position set in the second step. Thus, when the fifth step is performed, each variable value may correspond to a test range value set in the first step or to a measurement value set in the fourth step. This claim language is not indefinite, and thus, claims 4 and 5 should not be rejected under Section 112. (Claim 5 was rejected as depending from claim 4.) Also, claim 4 is amended to further support this point. It is respectfully believed that the claims are in compliance with section 112, and reconsideration of and withdrawal of the rejection is respectfully requested.

Claims 1-5 are rejected as being anticipated by U.S. Pat. No. 5,978,573 ("Ohara") under 35 U.S.C. §102(b). The Examiner's position is that Ohara discloses a semiconductor device testing method and apparatus that teaches all of the limitations in each of claims 1 through 5. Applicant respectfully traverses.

Ohara does not even disclose a semiconductor testing device or a testing device for detecting a pass/fail threshold or one that detects such a threshold using the method of applicant's claims. Instead, Ohara discloses a logic circuit design method for designing low-power SIC (semiconductor integrated circuit)

devices with no increase in the delay time of critical paths contained in CCs (combinational circuits) of an SIC. The method involves parsing a combination logic circuit into a low voltage section (with its circuit elements powered by a low voltage source) and a high voltage section (with its circuit elements powered by a higher voltage source). It is beneficial to have circuit elements powered by lower voltage supplies in order to reduce power consumption. Unfortunately, circuit elements operate slower with such lower voltages. Essentially, Ohara uses a binary search method to identify and define a division within the combination circuit for these sections that results in a maximum number of circuit elements being mapped in the low voltage section without materially degrading the overall circuit speed by detrimentally including those devices that make up critical timing paths.

The Examiner cited several parts of Ohara asserting that they teach specific limitations of claims 1-5. However, applicant respectfully submits that these citations do not teach the claims. For example, the Examiner asserts that the phrase: "At step S19, each CC thus mapped is checked if it has a signal propagation delay above the DDUL. Every CC with an excess delay is extracted at step S20 for further processing. (Col. 13, lines 16-18)" in support of the Examiner's position that Ohara discloses a semiconductor testing device. However, what this language is referring to is the checking of a combination circuit

design to confirm that it does not have any critical paths with critically high propagation delay times. In Ohara, a semiconductor device is not tested. Rather, Ohara's method is directed to the analysis of a circuit design. The "checking" step is performed through computational analysis, but a physical device is not actually measured.

Also, the Examiner cites the phrase: "The second embodiment employs a binary search method in which the boundary between the front and rear sections of a CC (i.e., the boundary between a CCE to be mapped into a 3VCC and a CCE to be mapped into a 2VCC) is defined. (Col. 13, lines 3-7)" to support the Examiner's position that Ohara teaches the use of a binary search method for detecting a pass/fail threshold. Again, applicant respectfully submits that this does not teach or suggest what applicant is claiming. Ohara is not searching for a pass/fail threshold. Rather, this portion of the Ohara patent refers to Ohara's use of a binary search method to identify an optimal boundary between the 3V and 2V combination circuit sections.

Accordingly, Ohara is completely different from what is recited by applicant's claims. Ohara actually appears not to disclose any of the elements of claims 1 through 5, and therefore, it is respectfully asserted that Ohara does not anticipate or teach the claims, and that the claims therefore are allowable.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

In light of the above noted amendments and remarks, this application is believed in condition for allowance and notice thereof is respectfully solicited. The Examiner is asked to contact applicant's attorney at 503-224-0115 if there are any questions.

Respectfully submitted,

James H. Walters, Reg. No. 35,731

Customer number 802
DELLETT AND WALTERS
Suite 1101
310 S. W. Fourth Avenue
Portland, Oregon 97204 US
(503) 224-0115
DOCKET: A-392

Certification of Facsimile Transmission

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MARKUP VERSION TO SHOW CHANGES MADE

In the Specification:

Replace the abstract paragraph with the following:

[The] In a semiconductor device testing apparatus and [the] test method [are disclosed whereby], after a pass value and fail value corresponding respectively to an upper limit and a lower limit of a test range have been set, measurement is not performed at these positions, but measurement is performed by means of a binary search method from the next position.

In the Claims:

4. (Amended) A semiconductor device test method for detecting a pass/fail threshold within a prescribed test range for a semiconductor device based on a binary search method, comprising:

a first step of setting either an upper-limit value or a lower-limit value of said test range as a pass value and the other limit value as a fail value;

a second step of setting a measurement position in accordance with the binary search method, using said pass value and said fail value;

a third step of performing a prescribed measurement on said semiconductor device at said measurement position set in said second step;

a fourth step of setting said [measurement position set in said second step as said] pass value equal to the measurement position set in said second step if the measurement result obtained in said third step is a pass, or setting said [measurement position set in said second step as said] fail value equal to the measurement position set in said second step if said measurement result is a fail; and

a fifth step of calculating a difference between said pass value and said fail value after a processing in said fourth step is completed, and giving a command to repeat the processing from said second step onward until this difference is equal to or less than a measurement resolution.